Amendments to the Claims:

Please cancel claims 2, 3, 7, and 8. Please amend claims 1, 4, 6, and 9 as follows.

The listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A clock and data recovery circuit comprising:

a clock signal generator [[for]]that generates[[ing]] ~~a plurality of~~ N clock signals, each clock signal having a phase difference[[t]] ~~phase~~ of 360/N degrees from each other, wherein N denotes an integer, and wherein phases of the N clock signals are 360/N x K, ~~with respect to the others~~ wherein K denotes an integer from K=0 to N-1;

a phase selector [[for]] that selects[[ing]] an $(I+2)_{th}$ ~~one of the~~ clock signal[[s]] of the ~~plurality of~~ N clock signals as a recovered clock signal if an ~~first~~ I_{th} clock signal of the ~~plurality of~~ N clock signals is in a first state and if an ~~second~~ $(I+1)_{th}$ clock signal of the ~~plurality of~~ N clock signals is in a second state when a logic level transition of a received data is detected, wherein I denotes an integer from 1 to N; and

a recovered data generator [[for]]that receives the received data and the recovered clock signal to generate[[ing]] a recovered data that is synchronized with the recovered clock signal output from the phase selector~~, using the received data~~.

2. – 3. (Canceled)

4. (Currently Amended) The clock and data recovery circuit according to claim [[3]]1, wherein the phase selector comprises:

N flip-flops for receiving the N clock signals and generating N clock signals and N complementary clock signals when a level transition of the received data is detected;

N AND gates for performing an AND operation of an I_{th} complementary clock signal and an $I+1_{th}$ clock signal out of the N clock signals and the N complementary clock signals; and

N switches for generating the $I+2_{th}$ clock signal as the recovered clock signal in response to corresponding output signals of the N AND gates.

5. (Original) The clock and data recovery circuit according to claim 4, wherein the recovered data generator receives the received data and generates the recovered data in response to the complementary signal of the recovered clock signal.

6. (Currently Amended) A method for recovering clock and data information from a signal comprising:

generating a plurality of clock signals, each clock signal having a phase difference[[t]] ~~phase~~ of 360/N degrees from each other, wherein N denotes an integer, and wherein phases of the N clock signals are 360/N x K, ~~with respect to the others~~ wherein K denotes an integer from K=0 to N-1;

selecting an $(I+2)_{th}$ ~~one of the~~ clock signal[[s]] of the ~~plurality of~~ N clock signals as a recovered clock signal if an ~~first~~ I_{th} clock signal of the ~~plurality of~~ N clock signals is in a first state and if an ~~second~~ $(I+1)_{th}$ clock signal of the ~~plurality of~~ N clock signals is in a second state when a logic level transition of a received data is detected, wherein I denotes an integer from 1 to N; [[,]] and

receiving the received data and the recovered clock signal to generate[[ing]] [[a]] the recovered data that is synchronized with the recovered clock signal ~~output from the phase selector, using the received data~~.

7. – 8. (Canceled)

9. (Currently Amended) The method according to claim [[8]]6, wherein the step of generating the recovered clock signal comprises steps of:

generating N clock signals and N complementary clock signals by receiving the N clock signals when a level transition of the received data is detected;

generating N AND operation signals by performing an AND operation of an I_{th} complementary clock signal and an $I+1_{th}$ clock signal out of the N clock signals and the N complementary clock signals; and

generating an $I+2_{th}$ clock signal as the recovered clock signal in response to the N AND operation signals.

10. (Original) The method according to claim 9, wherein the step of generating the recovered data generates the recovered data by using the received data in response to a complementary signal of the recovered clock signal.